

REMARKS

Claim Rejections -35 USC §112

The rejection includes:

"Claims 63, 67, 72, 77, 81, and- 86 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim-the subject matter which applicant regards as the invention.

Regarding claim 63, lies 2-4 isunclear. What does applicant mean of "second edge of the trace and first edge of the second cap are both substantially equal to X"? Does applicant mean either the dimension or size of the second edge of the trace and -the first edge of the second cap are both substantially equal to X (0.1 in).

Rejected claims 67, 72, 77, and 88 are similar to claim 63.

Please clarify."

The issue raised by the Examiner seeks the meaning of a claim phrase. It is submitted that the language quoted is already clear when considered in the context in which it appears particularly by referring to Figure 1 of the drawing.

The entire claim 63 is:

63. The circuit protection system as described in claim 62 wherein **the dimension of the space intermediate**

- (1) said first edge of said trace and said first edge of said first end cap and
- (2) said second edge of said trace and said first edge of said second end cap

are both substantially equal to X. (emphasis added)

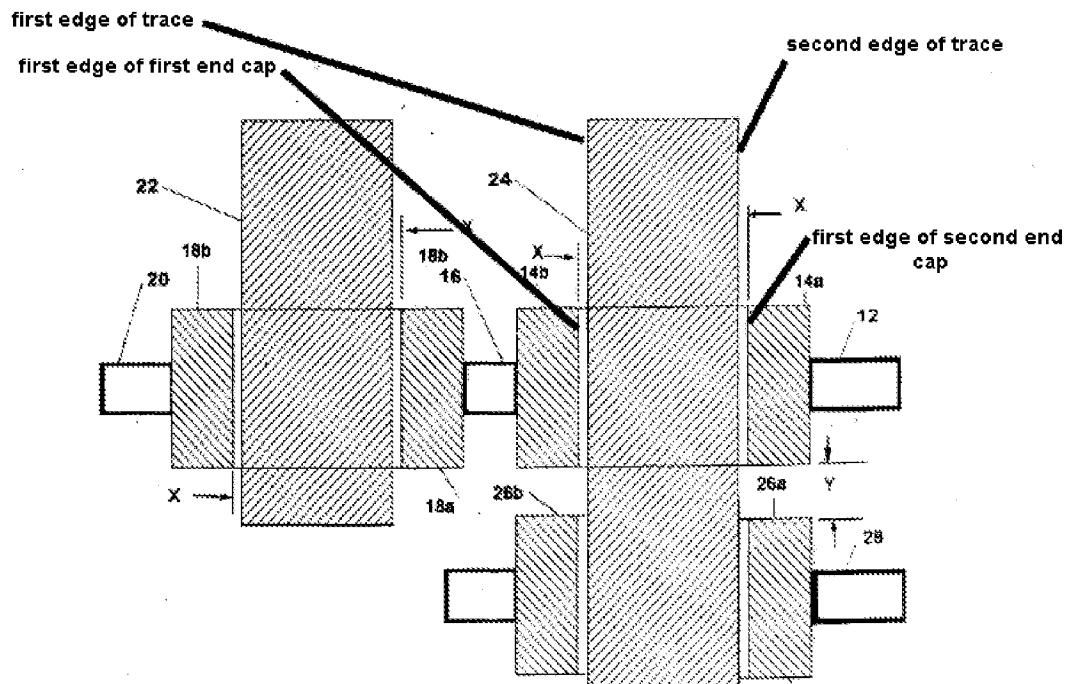


FIG. 1

The marked up copy of Fig. 1 of the drawing above is provided to emphasize that which is shown in the drawing including the explicitly labeled dimension. It will be understood that "X" is used to refer the dimension of the space intermediate both a first set of two edges as well as the dimension of the space intermediate a second set of two edges.

The term "X" is used in the same sense that it is used in elementary algebra. See
<http://www.newton.dep.anl.gov/askasci/math99/math99228.htm>
<http://www.garlikov.com/math/UnderstandingAlgebra.html>

As used in claim 63 the dimension is an unspecified quantity, however, the claims make clear that both of the respective dimensions are substantially equal to X. Thus, the first and second dimensions are inherently substantially equal to each other. The use of the standard algebraic representation in claim 63 facilitates subsequent more specific claims. Claim 63 further limits claim 62 because it specifies that two specific dimensions are substantially equal. Claim 65 is a more specific claim that specifies that the two recited dimensions are both substantially equal to each other and substantially equal to .01 inch.

It is respectfully submitted that the asserted issue relates to specific words out of the context in which they appear. The words when taken in context are fully supported by both the original specification and the specification as amended in the response dated 10/11/06 that included:

The meaning of the words is most apparent by consideration of page 8 of the specification.

Claim Rejections -35 USC §102

The rejection is:

5. Claims 62-70,76-84 are rejected under 35 U.S.C. 102(e) as being anticipated by Devoe (U.S. Patent 6,690,558)

As to claims 62, 76, Devoe discloses a high power resistor device (30; 40) as shown in figures 3A-3C comprising:

a printed circuit board (48, column 4, line 24) having a SMT component (30; 40) mounted on, the component (30; 40) having first and second end caps (14), and each caps having a first edge;

a conductive trace (46, see figure 3C) formed on the PCB (48) having first and second opposed edges extending intermediate said first and second caps (14), the edges of the trace (46) being defined a plane, see figure 3C and intersecting the first edge of the first cap (14) and intersecting the first edge of

the second cap (14), the edge of the trace (46) disposed in parallel spaced relative to the edge of the first and second caps respectively.

As to claims 66,80, Devoe discloses a high power resistor device (30; 40) as shown in figures 3A-3C comprising:

a printed circuit board (48, column 4, line 24) having first and second SMT components (30,40) mounted on, the components (30, 40) having first and second end caps (14), and each caps having a first edge; a conductive trace (46, see figure 3C) formed on the PCB (48) having first and second opposed edges extending intermediate said first and second caps (14), the edges of the trace (46) being defined a plane, see figure 3C and intersecting the first edge of the first cap (14) and intersecting the first edge of the second cap (14), the edge of the trace (46) disposed in parallel spaced relative to the edge of the first and second caps respectively, and said plane intersecting said first edge of said first end cap of said second surface mounted component (40) and intersecting said first edge of said second end cap of said second surface mounted component, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap of said second surface mounted component and said second edge of said trace being disposed in parallel spaced (sic)

Regarding claims 63-65, 67-70, 77-79, and 81-84, Devoe discloses the second edge of the trace being substantially the same to the first edge of the second cap.

Each independent claim in the rejected claims includes the following:

"...a conductive trace on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps, said first and second opposed edges being coplanar and thereby defining a plane, said plane intersecting said first edge of said first end cap and intersecting said first edge of said second end cap, said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap ..." (emphasis added)

The following is a marked copy of Devoe Fig. 3C in which a bold horizontal line represents the plane defined by the edges of the two discrete traces 46, 46.

U.S. Patent Feb. 10, 2004 Sheet 2 of 3 US 6,690,558 B1

PLANE DEFINED BY EDGES OF TRACES 46, 46

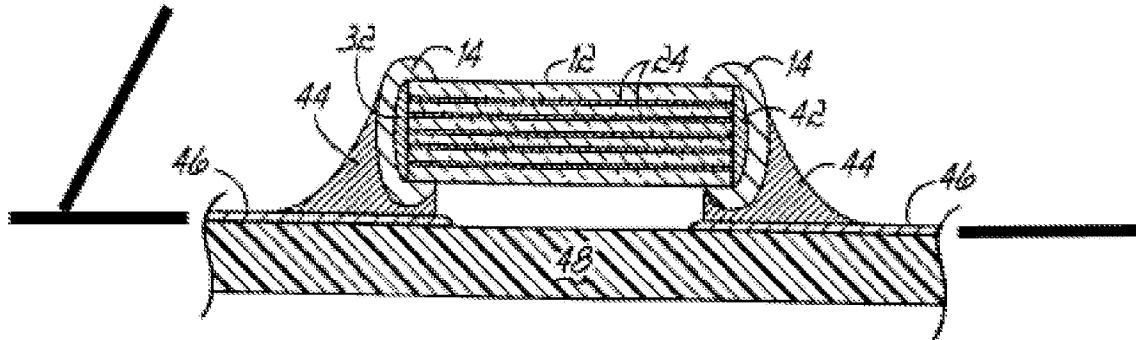


FIG. 3C

The trace 46 in Devoe is not coplanar with the end caps. The plane defined by the edges of the trace do not intersect the end caps. The trace does not extend intermediate end caps. Instead, the trace extends in a plane at a lower elevation. Thus, the reference does not have the same structure. In addition the trace 46 is attached to the end caps by solder and thus does not have a spacing that is necessary for the function of present invention. Furthermore, the trace in Devoe is used to connect the device to the board. Any surge will inherently pass through that trace. Thus, the traces 46, 46 in Devoe are the source of transients not a protection from transients!

The above is summarized in the following table:

THE PARSED CLAIM with reference numerals added	THE REFERENCE	COMMENT
62. A circuit protection system for dissipating transients without the use of transorbs or metal oxide varistors which comprises:		
a printed circuit board;		
a surface mount component mounted on said printed circuit board, said surface component having first and second end caps, said first and second end caps each having a first edge;		
a conductive trace 24 on said printed circuit board having first and second opposed edges extending intermediate said first and second end caps,	The rejection asserts element 46 of the reference meets the claim.	Element 46 of the reference is not intermediate the end caps 14, 14 of the reference3,. The specification of the reference makes clear at column 4, lines 3-4 that the respective end caps of the 14, 14 of the resistor 32 are joined to respective traces (plural not singular) on the substrate 48. The reference has no trace intermediate the end caps .
said first and second opposed edges being coplanar and thereby defining a plane,	The elements 46, 46 do have edges that could define a plane	
said plane intersecting said first edge of said first		A plane defined by the elements 46, 46 does

end cap and intersecting said first edge of said second end cap,		not intersect any part of any end cap 14
said first edge of said trace being disposed in parallel spaced relation to said first edge of said first end cap and said second edge of said trace being disposed in parallel spaced relation to said first edge of said second end cap.		The respective traces are physically and electrically connected to the end caps! Thus, they clearly are not disposed in spaced relation much less in parallel spaced relation to the end caps.

Thus, the reference does not have the structure explicitly claimed, the purpose of the invention either intended or implicitly, and does not achieve the result of the present invention either intentionally or inherently. Accordingly, there is no rational, good faith, plausible, or credible support for rejection based on the cited reference.

The allowed claims are again noted.

It is respectfully submitted that the now rejected claims (including withdrawn claims) are allowable and such action is requested.

Should a petition for an Extension of Time be necessary for the timely reply to the outstanding office action (or such a petition has been made and an additional extension is necessary) petition is hereby made in the Commissioner is

authorized to charge any fees (including additional claim fees) to Deposit Account Number 19-2635 under Attorney Docket Number H0006069-0555.

Respectfully submitted,



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03/10/2008

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